a computer connectable to the boundary scan test port, the computer having a boundary scan description language file, a netlist, and a connections list loaded therein, the computer being adapted to compile these into a data structure for testing a circuit on the board and to receive a test script specific to an integrated circuit mounted on the board and to run the test script using the data structure to thereby send to the boundary scan test port selected signals to test selected pins of the integrated circuit.

24. (Newly added) The equipment of claim 23, wherein the test script is specific to the integrated circuit to be tested but independent of the circuit board on which it is mounted.

25. (Newly Added) The circuit testing equipment according to claim 1, wherein the test script is also associated with other electrical components to be tested, including at least one of switches and light emitting diodes.

REMARKS

I. 35 U.S.C § 112

Applicant submits that the enclosed amendments addrsse the Examiner's rejection of the claims under 35. U.S.C. § 112 (second paragraph).

35 U.S.C. §.103

The following remarks show that the claimed invention is not suggested by any of the references cited and there is no motivation to modify any of the references to arrive at the invention for the following reasons.

US 6.012,155 - *Beausang el al*

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This document teaches no more than how to produce a BSDL file for a given chip. *Beausang* teaches no more than how to produce the BSDL file from the hardware description language of a chip which has JTAG capability. The BSDL file is necessary to know how to control JTAG aspects of the chip. This is a starting point for producing one of the BSDL files 111 of Fig 2 of the present application. It is assumed in the description of the present invention that these files are supplied by the supplier of the chip to be tested.

US 6.539,520 Bl *of Tiong et al*

This document describes something similar to *Beausang*. *Tiong* describes a sort of Internet service which allows a user to describe some connections and produces a hardware description language. It also describes how it can generate a BSDL file. It is very similar to the teaching of *Beausang* in that the end result is a BSDL file.

US 6.988.239 of *Folea.*

Referring to column 2, lines 43 to 51, it is explicitly explained:

> *"The present invention overcomes the above noted issues of the prior an by providing a method and apparatus that does not require the use of test vectors, text executives, net lists, or schematics to run boundary scan operations...".*

The Examiner concedes that a net list and a connections list are not explicitly disclosed by *Folea*. It is correct that *Folea* makes no mention and does not suggest the use of a connections list. Moreover *Folea* explicitly teaches away from including or using a net list. Given that *Folea* teaches away from the use of a net list, it cannot be said that it would be obvious to refer to any other reference to include the feature which *Folea* explicitly seeks to avoid. Neither would it have

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been obvious to further include a connections list, where *Folea* explicitly teaches away from using even a net list.

US 6,757,844 *Lulla et al*

Column 2, lines 50 to 59, describe how the circuit 100 of *Lulla* comprises two dies in a single integrated circuit package or two chips on a circuit board. Note that, in the case of two chips on an integrated circuit package, there would be a single BSDL file for the entire chip. Note that this is still true for two chips on a circuit board. There would be a single BSDL file for the circuit board. There is no suggestion in *Lulla et al* of providing separate BSDL files, a net list and connections list and passing these three items to generate a data structure which, when combined with a test script, permits execution of the test script from the computer through the boundary scan bus. To the contrary, the entire description relates to a specific combination of a JTAG die and a memory die and control (in operation) of the memory die through the JTAG port.

Referring to column 1, lines 33 to 55, it can be seen that the problem addressed by *Lulla et al* is the provision of additional memory (volatile or non-volatile), without having to provide extra pins to program the memory (lines 49 to 51). To overcome this problem and provide additional memory without additional pins or additional programming circuitry, the author has described the use of the JTAG bus to control a memory that does not have JTAG support. There is no description of any test mode of operation. The entire description is of an operational mode in which the JTAG bus is used in this unusual manner, rather than for its usual test purposes.

Lulla et al is not concerned with running test scripts. Accordingly, there is no suggestion in *Lulla* of providing a BSDL file, a net list and a connections list and passing these to generate a data structure which, when combined with the test script, permits execution of a test script from a

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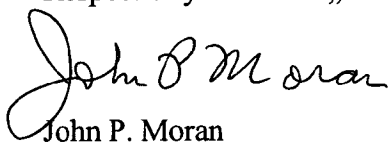
computer through the boundary scan bus.

There is no teaching or suggestion of providing circuit testing equipment, for testing the described circuit, comprising an input for inputting files comprising a boundary scan description language (BSDL) file, a netlist and a connections list. There is no teaching or suggestion of generating a data structure generated from the BSDL file, the netlist and the connections list that defines all pins of the first IC that are capable of driving pins of the second IC and all pins of the first IC that are capable of reading pins of the second IC, whereby the second IC and its connections to the first IC can be tested by driving pins of the first IC using a test script. There is no teaching or suggestion of any test script that is specific to the second IC but independent of the first IC.

If any additional fee is required in connection with this Preliminary Amendment, Applicants requests that such fee be charged to Deposit Account No. 502353.

Respectfully submitted,,



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